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AUG 16 2004

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	10/645,201
Filing Date	21-Aug-2003
First Named Inventor	Jade M. Kizer
Group Art Unit	2661
Examiner Name	Douglas W. Olms

Attorney Docket Number RBUS 1305-1

U.S. PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
JK	A50	5,548,146		Kuroda et al.	08-20-1996	
JK	A51	6,377,640		Trans	04-23-2002	
	A3					
	A4					
	A5					
	A6					
	A7					
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	A9					
	A10					
	A11					
	A12					
	A13					
	A14					
	A15					
	A16					
	A17					
	A18					
	A19					
	A20					

FOREIGN PATENT DOCUMENTS

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		Office ³	Number ⁴				
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	B2						
	B3						
	B4						
	B5						
	B6						
	B7						
	B8						
	B9						
	B10						

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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	10/645,201
(use as many sheets as necessary)		Filing Date	21-Aug-2003
Sheet	2	First Named Inventor	Jade M. Kizer
	of	Group Art Unit	2661
	2	Examiner Name	Douglas W. Ulms
		Attorney Docket Number	RBUS 1305-1

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
<i>MKJ</i>	C27	WIDMER, A.X., et al., "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM J. Res. Develop., Vol. 27, No. 5, September 1983, 440-451.	
	C28	BANU, MIHAI, et al., "TA 6.4: A 660Mv/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ Data and Burst-Mode Transmission," IEEE International Solid State Circuits Conference, 1993, 102-103, 270.	
	C29	ELDERING, CHARLES A., et al., "Digital Burst Mode Clock Recovery Technique for Fiber-Optic Systems," Journal of Lightwave Technology, Vol. 12, No. 2, February 1994, 271-279.	
	C30	CHANG, KEN K. Y., et al., "A 2 Gb/s Asymmetric Serial Link for High-Bandwidth Packet Switches," Hot Interconnects V, Stanford University, August 1997, 1-9.	
	C31	HU, TIMOTHY H., et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2- CMOS," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, 1314-1320.	
	C32	KIM, SUNGJOON, et al, "An 800Mbps Multi-Channel CMOS Serial Link with 3x Oversampling," IEEE 1995 Custom Integrated Circuits Conference, 22.7.1-22.7.4.	
	C33	NAKAMURA, KAZUYUKI, et al., "A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock," 1998 Symposium on VLSI Circuits Digest of Technical Papers, 196-197.	
	C34	POULTON, JOHN, et al., "A Tracking Clock Recovery Receiver for 4Gb/s Signaling, Hot Interconnects '97, August 21-23, 1997, Palo Alto, CA, 1-13.	
	C35	DALLY, W., et al., "DIGITAL SYSTEMS ENGINEERING," Cambridge University Press, 1998, pages 447-449.	
<i>MKJ</i>	C36	CERISOLA, M., et al., "CORD - a WDM Optical Network: Control Mechanism Using Subcarrier Multiplexing and Novel Synchronization Solutions," Communications, 1995. ICC 95 Seattle, Gateway to Globalization, 1995 IEEE International Conference on , Volume: 1 , 18-22 June 1995 Pages:261 - 265 vol.1	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1

of

4

Complete if Known

Application Number	10/645,201
Filing Date	21 August 2003
First Named Inventor	Jade M. Kizer
Group Art Unit	2816 2661
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1305-1

U.S. PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
MK	A1	3,155,102		Niederer, Jr. et al.	11-03-1964	
MK	A2	3,638,121		Spilker, Jr.	01-25-1972	
MK	A3	3,922,491		Bjork et al.	11-25-1975	
MK	A4	4,648,133		Vilnrotter	03-03-1987	
MK	A5	5,243,626		Devon et al.	09-07-1993	
MK	A6	5,485,490		Leung et al.	01-16-1996	
MK	A7	5,511,091		Saito	04-23-1996	
MK	A8	5,523,760		McEwan	06-04-1996	
MK	A9	5,554,945		Lee et al.	09-10-1996	
MK	A10	5,621,913		Tuttle et al.	04-15-1997	
MK	A11	5,742,798		Goldrian	04-21-1998	
MK	A12	6,369,652		Nguyen et al.	04-09-2002	
MK	A13	6,421,389		Jett et al.	07-16-2002	
MK	A14	6,606,350		Dress, Jr. et al.	08-12-2003	
MK	A15	6,657,468		Best et al.	12-02-2003	
MK	A16	6,690,741		Lerrick, Jr. et al.	02-10-2004	
MK	A17	6,717,992		Cowie et al.	04-06-2004	
MK	A18	2001/0048382		Low et al.	12-06-2001	
MK	A19	2001/0053175		Hector et al.	12-20-2001	
MK	A20	2003/0063597		Suzuki	04-03-2003	

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		Office ³	Number ⁴	Kind Code ⁵ (If known)				
MK	B1	JP	02000035831A		Nitsusan Jidosha KK	08-14-1990	Abstract only	
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	B3							
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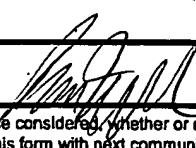
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/645,201
Sheet	2	of	4	Filing Date	21 August 2003
				First Named Inventor	Jade M. Kizer
				Group Art Unit	2816 2661
				Examiner Name	Unassigned
				Attorney Docket Number	RBUS 1305-1

U.S. PATENT DOCUMENTS					
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Ma	A21	2003/0146800	Dvorak	08-07-2003	
Ma	A22	2003/0198212	Hoctor et al.	10-23-2003	
Ma	A23	2003/0198308	Hoctor et al.	10-23-2003	
Ma	A24	2004/0032354	Knobel et al.	02-19-2004	
Ma	A25	2004/0057500	Balachandran et al.	03-25-2004	
	A26				
	A27				
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	A36				
	A37				
	A38				
	A39				
	A40				

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	B11				
	B12				
	B13				
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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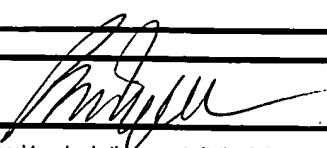
Sheet 3 of 4

Complete if Known

Application Number	10/645,201
Filing Date	21 August 2003
First Named Inventor	Jade M. Kizer
Group Art Unit	2816
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1305-1

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
<i>JK</i>	C1	ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."	
	C2	ZERBE, JARED ET AL, U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."	
	C3	U.S. Patent Application No. 10/278,708 filed 22 October 2002, entitled "Phase Adjustment Apparatus and Method for a Memory Device Signaling System."	
	C4	DANIELE, N. et al., "Principle and Motivations of UWB Technology for High Data Rate WPAN Applications," SOC 2003, 4 pages.	
	C5	WIN, MOE Z., et al., "Impulse Radio: How it Works," IEEE Communications Letters 2(2), Feb. 1998, 36-38.	
	C6	DANIELE, NORBERT, "Ultra Wide Band Principles and Applications for Wireless Communications," CEA-LETI Annual Review, 25 and 26 June 2002, 24 pages.	
	C7	U.S. Patent Application No. 09/941,079 filed 28 August 2001 entitled "Clock Data Recovery with Selectable Phase Control Input."	
	C8	Yang, Chih-Kong Ken "Design of High-Speed Serial Links in CMOS" Technical Report No. CSL-TR-98-775, Sponsored By Center for Integrated Systems, Sun Microsystems and LSI Logic Inc. December 1998, pp. 1-182.	
	C9	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SDRAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.	
	C10	GILLINGHAM, PETER, "SDRAM Architectural and Functional Overview," SDRAM Consortium (29 Aug 1997), 1-14.	
<i>JK</i>	C11	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages	

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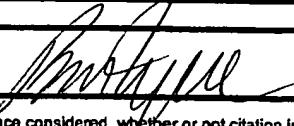
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Sheet	4	of	4	Filing Date	21 August 2003
				First Named Inventor	Jade M. Kizer
				Group Art Unit	2816
				Examiner Name	Unassigned
				Attorney Docket Number	RBUS 1305-1

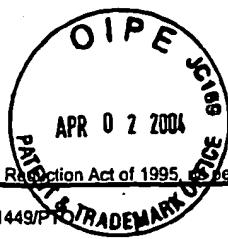
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
<i>JK</i>	C12	GILLINGHAM, PETER, "SLDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39
	C13	SLDRAM Inc., "400 Mb/s/pin SDRAM," Draft Advance (9 Jul 1998), 1-69.
	C14	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages
	C15	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages
	C16	INTEL "How to Measure RDRAM® System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15
	C17	CHANG, KUN YUNG "Design of a CMOS Asymmetric Serial Link" A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University August 1999, 119 pages
<i>JK</i>	C18	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages
	C19	
	C20	
	C21	

Examiner Signature		Date Considered	5/31/05
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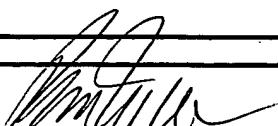
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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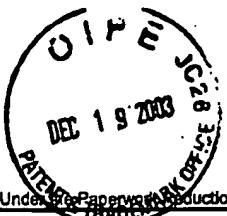
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				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket Number	RBUS 1305-1

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
<i>JK</i>	C1	U.S. Patent Application No. 10/278,478, Filed 22 October 2002 entitled "Timing Calibration Apparatus and Method for a Memory Device Signaling System"			
<i>JK</i>	C2	Chang, Kun-Yung "Design of a CMOS Asymmetric Serial Link" A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University August 1999, 119 pages			

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

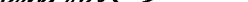
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Sheet 1

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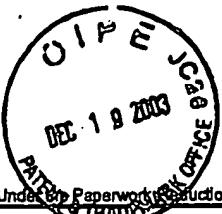
Application Number	10/645,201
Filing Date	21 August 2003
First Named Inventor	Jade M. Kizer
Art Unit:	Unknown 2661
Examiner Name	Unknown
Attorney Docket Number	RBUS 1305-1

Examiner Signature		Date Considered	5/31/05
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INFORMATION DISCLOSURE
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Sheet

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Complete If Known

Application Number	10/645,201
Filing Date	21 August 2003
First Named Inventor	Jade M. Kizer
Art Unit	Unknown
Examiner Name	Unknown

Attorney Docket Number RBUS 1305-1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
BN	C1	SLDRAM Inc. "400 Mb/s/pin SDRAM" 4M x 18 SDRAM, July 9, 1998, pp. 1-69	
BN	C2	Peter Gillingham "SLDRAM Architectural and Functional Overview" August 29, 1997, pp. 1-14	
BN	C3	Peter Gillingham et al. "SLDRAM: High-Performance, Open-Standard Memory" IEEE November/December 1997, pp. 29-39	
BN	C4	Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society "Draft Standard for a High-Speed Memory Interface (SyncLink)" 1996 pp. 1-56	
BN	C5	Direct Rambus Short Channel Layout Guide August 2001, pp. 1-40	
BN	C6	Direct Rambus Long Channel Design Guide, 2000, pp. 1-45	
BN	C7	How to Measure RDRAM* System Clock Jitter, Intel June 1999, pp. 1-15	
BN	C8	Lluis Paris et al. "WP 24.3 A 800MB/s 72 Mb SDRAM with Digitally-Calibrated DLL" IEEE International Solid-State Circuits Conference 1999., pp 1-5	
BN	C9	Yasunobu Nakase et al. "Source-Synchronization and Timing Vernier Techniques for 1.2 GB/s SDRAM Interface" IEEE Journal of Solid-State Circuits, Vol. 34, No. 4, April 1999	
BN	C10	RDRAM Direct Rambus Clock Generator, April 2002, pp. 1-22	

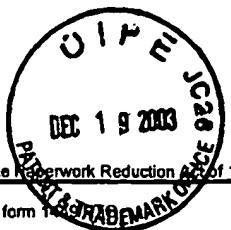
Examiner Signature		Date Considered	5/31/05
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Sheet 3 of 3 Attorney Docket Number RBUS 1305-1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	
Filing Date	21 August 2003 (herewith)
First Named Inventor	Jade M. Kizer
Group Art Unit	2661
Examiner Name	

Attorney Docket Number RBUS 1305-1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
A1	6,282,210			Rapport et al.	08-28-2001	
A2	6,359,931			Perino et al.	03-19-2002	
A3	6,396,329			Zerbe	05-28-2002	
A4	6,448,815			Talbot et al.	09-10-2002	
A5	6,469,555			Lau et al.	10-22-2002	
A6	6,473,439			Zerbe et al.	10-29-2002	
A7	6,539,072			Donnelly et al.	03-25-2003	
A8						
A9						
A10						
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number	
		Filing Date	21 August 2003 (herewith)
		First Named Inventor	Jade M. Kizer
		Group Art Unit	
		Examiner Name	
Sheet	2	of	2
		Attorney Docket Number	RBUS 1305-1

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (In CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>BN</i>	C1	RaSer™ X Product Brief, "Highly Flexible 10 Gbps Backplane Serial Link Interface," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
<i>BN</i>	C2	Yellowstone Technology Brief, "High Performance Memory Interface Technology," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
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<i>BN</i>	C5	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte," National Semiconductor, National Edge (Sep. 2001) 5 pages, http://www.national.com/nationaledge/sep01/864.html .	

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Sheet

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of

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Application Number	10/645,201
Filing Date	21 August 2003
First Named Inventor	Jade M. Kizer
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		Number	Kind Code ² (if known)			
JK	A1	5,122,978		Merrill	06-16-1992	
JK	A2	5,436,908		Fluker et al.	07-25-1995	
JK	A3	6,219,384		Kliza et al.	04-17-2001	
JK	A4	6,463,392		Nygaard et al.	10-08-2002	
JK	A5	6,510,503		Gillingham et al.	01-21-2003	
JK	A6	6,556,934		Higashide	04-29-2003	
JK	A7	2001/0056332		Abrosimov et al.	12-27-2001	
JK	A8	2002/0072870		Adam et al.	06-13-2002	
JK	A9	2002/0138224		Sessions	09-26-2002	
	A10					
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		Office ⁴	Number ⁵	Kind Code ⁶ (if known)				
	B1							
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Signature

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